WF88-AW

Wi-Fi Aware Module

Amp’ed RF Technology, Inc.

www.ampedrftech.com

WF88-AW Product Specification

Description

Amp'ed RF Tech presents the WF88, a compact dual-band (2.4/5 GHz) Wi-Fi IoT module engineered for rapid product integration and scalable wireless connectivity.

The WF88 supports IPv6, mesh networking, and Wi-Fi Aware (NAN), enabling both infrastructure-based and direct device-to-device communication. Delivering up to 300 meters line-of-sight range, the WF88 reduces development complexity while providing a flexible platform for next-generation IoT applications.

Typical applications include:

- Wi-Fi Aware (NAN) proximity-based services
- Remote metering and AMR systems
- Secure device onboarding and private networks
- Mesh networking and distributed IoT systems
- Smart home automation and control
- Industrial monitoring and control

Features

Hardware

- Dual-core CA32 Processor
- WF88-AW: 24mm x 20mm
- UART/SD/USB/SPI

WLAN

- 802.11a/b/g/n/ac/ax
- Dual Band: 2.4/5GHz
- WiFi Aware
- Output Power, +20dBm
- Security: WAP1~WPA3
- OTAP support
- Support firmware updates via USB flash drive

Contents

1. Hardware Specifications

General Conditions 25°C

1.1. Recommended Operating Conditions

Rating	Min	Typical	Max	Unit
Operating Temperature Range	-40	-	+85	°C
Supply Voltage VDD	4.5	5	5.5	Volts
Signal Pin Voltage	-	3.3	-	Volts
RF Frequency for 2.4G	2412	-	2484	MHz
RF Frequency for 5G	5180		5885	MHz

1.2. Absolute Maximum Ratings

Rating	Min	Typical	Max	Unit
Storage temperature range	-55	-	+105	°C
Supply Voltage VDD	-0.3	-	+8	Volts
I/O pin voltage VIO	-0.3	-	+3.63	Volts
RF input power	-	-	-5	dBm

1.3. I/O Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low-Level Input Voltage	-	0.8	Volts
V_{IH}	High-Level Input Voltage	2.0	-	Volts
V_{OL}	Low-Level Output Voltage	-	0.5	Volts
V_{OH}	High-Level Output Voltage	2.8	-	Volts
I_{OL}	Low –Level Output Current	-	4.0/8.0	mA
I_{OH}	High-Level Output Current	-	4.0/8.0	mA

1.4. Current Consumption

VDD=5V	Avg	Unit
Standby	82	mA
Active	95	mA
Ipeak: system maximum peak current draw	350	mA

1.5. Selected RF Characteristics

Parameters	Conditions	Typical	Unit
Antenna load		50	ohm
Wi-Fi Receiver 2.4 GHz 11b			
Sensitivity	1Mbps CCK	-100	dBm
Sensitivity	2Mbps CCK	-96	dBm
Sensitivity	5.5Mbps CCK	-94	dBm
Sensitivity	11Mbps CCK	-90	dBm
Wi-Fi Receiver 2.4GHz 11g			
Sensitivity	BPSK rate 1/2, 6Mbps OFDM	-95	dBm
Sensitivity	BPSK rate 3/4, 9Mbps OFDM	-94	dBm
Sensitivity	QPSK rate 1/2, 12Mbps OFDM	-92	dBm
Sensitivity	QPSK rate 3/4, 18Mbps OFDM	-89	dBm
Sensitivity	16-QAM rate 1/2, 24Mbps OFDM	-86	dBm
Sensitivity	16-QAM rate 3/4, 36Mbps OFDM	-83	dBm
Sensitivity	64-QAM rate 1/2, 48Mbps OFDM	-79	dBm
Sensitivity	64-QAM rate 3/4, 54Mbps OFDM	-77	dBm
Wi-Fi Receiver 2.4GHz 11n BW=20MHZ			
Sensitivity	MCS0,BPSK rate 1/2	-95	dBm
Sensitivity	MCS1,QPSK rate 1/2	-92	dBm
Sensitivity	MCS2,QPSK rate 3/4	-89	dBm
Sensitivity	MCS3,16-QAM rate 1/2	-86	dBm
Sensitivity	MCS4,16-QAM rate 3/4	-82	dBm
Sensitivity	MCS5,64-QAM rate 2/3	-78	dBm
Sensitivity	MCS6,64-QAM rate 3/4	-77	dBm
Sensitivity	MCS7,64-QAM rate 5/6	-75	dBm
Wi-Fi Receiver 2.4GHz 11ax BW=20MHZ			
Sensitivity	MCS0,BPSK rate 1/2	-93	dBm
Sensitivity	MCS1,QPSK rate 1/2	-90	dBm
Sensitivity	MCS2,QPSK rate 3/4	-88	dBm
Sensitivity	MCS3,16-QAM rate 1/2	-85	dBm
Sensitivity	MCS4,16-QAM rate 3/4	-82	dBm

Sensitivity	MCS5,64-QAM rate 2/3	-77	dBm
Sensitivity	MCS6,64-QAM rate 3/4	-76	dBm
Sensitivity	MCS7,64-QAM rate 5/6	-75	dBm
Sensitivity	MCS8,256-QAM rate 3/4	-71	dBm
Sensitivity	MCS9,256-QAM rate 5/6	-69	dBm
Wi-Fi Receiver 2.4GHz			
Output Power	HT20,MCS0,BPSK rate 1/2	20	dBm
Wi-Fi Receiver 5GHz 11a			
Sensitivity	BPSK rate 1/2,6Mbps OFDM	-94	dBm
Sensitivity	BPSK rate 3/4,9Mbps OFDM	-93	dBm
Sensitivity	QPSK rate 1/2,12Mbps OFDM	-92	dBm
Sensitivity	QPSK rate 3/4,18Mbps OFDM	-89	dBm
Sensitivity	16-QAM rate 1/2,24Mbps OFDM	-86	dBm
Sensitivity	16-QAM rate 3/4,36Mbps OFDM	-83	dBm
Sensitivity	64-QAM rate 1/2,48Mbps OFDM	-79	dBm
Sensitivity	64-QAM rate 3/4,54Mbps OFDM	-77	dBm
Wi-Fi Receiver 5GHz 11n/ac BW=20MHz			
Sensitivity	MCS0,BPSK rate 1/2	-94	dBm
Sensitivity	MCS1,QPSK rate 1/2	-91	dBm
Sensitivity	MCS2,QPSK rate 3/4	-89	dBm
Sensitivity	MCS3,16-QAM rate 1/2	-86	dBm
Sensitivity	MCS4,16-QAM rate 3/4	-82	dBm
Sensitivity	MCS5,64-QAM rate 2/3	-78	dBm
Sensitivity	MCS6,64-QAM rate 3/4	-77	dBm
Sensitivity	MCS7,64-QAM rate 5/6	-75	dBm
Wi-Fi Receiver 5GHz 11ac BW=20MHz			
Sensitivity	MCS8,256-QAM rate 3/4	-71	dBm
Wi-Fi Receiver 5Hz 11ax BW=20MHZ			
Sensitivity	MCS0,BPSK rate 1/2	-94	dBm
Sensitivity	MCS1,QPSK rate 1/2	-90	dBm
Sensitivity	MCS2,QPSK rate 3/4	-88	dBm

Sensitivity	MCS3,16-QAM rate 1/2	-85	dBm
Sensitivity	MCS4,16-QAM rate 3/4	-82	dBm
Sensitivity	MCS5,64-QAM rate 2/3	-78	dBm
Sensitivity	MCS6,64-QAM rate 3/4	-76	dBm
Sensitivity	MCS7,64-QAM rate 5/6	-75	dBm
Sensitivity	MCS8,256-QAM rate 3/4	-71	dBm
Sensitivity	MCS9,256-QAM rate 5/6	-69	dBm
Wi-Fi Transmitter 5GHz			
Output Power	HT20,MCS0,BPSK rate 1/2	19	dBm

1.6. Pin Assignment

Assignment	Type	Pin #	Description
GND		1	
VDD	P	2	Supply in 5V
USB_DP	I/O	3	USB positive differential signal
USB_DM	I/O	4	USB negative differential signal
NC		5	
UART2_RTS	I/O	6	UART2 RTS
UART2_CTS	I/O	7	UART2 CTS
UART2_TXD	I/O	8	UART2 TXD
UART2_RXD	I/O	9	UART2 RXD
LOG_RXD	I/O	10	
LOG_TXD/BOOT	I/O	11	1: Enter into normal boot mode 0: Enter into UART download mode
NC	I/O	12-13	
SD_CMD	I/O	14	Command
SD_CLK	I/O	15	Clock
SD_D0	I/O	16	Data Bit 0
SD_D1	I/O	17	Data Bit 1
SD_CD	I/O	18	Card Detect
SD_D2	I/O	19	Data Bit 2
SD_D3	I/O	20	Data Bit 3

SD_WP	I/O	21	SD Write Protect
UART0_RXD/SPI1_CS	I/O	22	The default function is SPI1.
UART0_TXD/SPI1_CLK	I/O	23	
UART0_CTS/SPI1_MISO	I/O	24	
UART0_RTS/SPI1_MOSI	I/O	25	
SPI0_MOSI	I/O	26	Master Out Slave In
SPI0_MISO	I/O	27	Master In Slave Out
SPI0_CLK	I/O	28	Serial Clock
SPI0_CS	I/O	29	Chip Select
RESET	RST	30	Chip enable. 1: Enable chip 0：Shut down chip
NC		31	
NC		32	
GND		33	

1.7. Functional Description

1.7.1 RESET

RESET is the enable pin of the WF88-AW, which can be used to reset the module. RESET pin has been pull high **with 10K resistor by default.**

If the chip needs to be rest through RESET pin, it is necessary to ensure that the RESET is pulled down by at least 0.1ms. If not controlled, keep the RESET pin floating.

1.7.2 Universal Asynchronous Receiver/Transmitter (UART, LOGUART)

The WF88-AW has embedded two general UART interfaces (UART1, UART2).

The UART offers a flexible means of full-duplex data exchange with external equipment, requiring an industry-standard NRZ asynchronous serial data format. It provides a very wide range of baud rates using a fractional baud rate generator.

The UART supports the following features:

- Various UART formats: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Baud rate 115.2 kbps up to 8Mbps
- Hardware Interface auto-flow control

The LOGUART is responsible for printing logs.

The LOGUART supports:

- Various UART formats: 1 start bit, 8 data bits, 0 parity bit and 1 stop bits
- 1.5Mbps baud rate for fast log printing

1.7.3 Serial Peripheral Interface (SPI)

The WF88-AW features two SPIs (SPI0, SPI1) that allow communication at up to 50Mbit/s in master and slave modes, in half-duplex, full-duplex and simplex modes. All SPI interfaces support hardware CRC calculation and 64X16-bit embedded Rx and Tx FIFOs with DMA capability.

The SPI has the following features:

- Two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps
- 8 bits data frame size
- Clock bit rate – Dynamic control of the serial bit rate of the data transfer, only when configured in Master Mode
- Configurable clock polarity
- Transfer mode: transmit and receive

1.7.4 Universal Serial Bus (USB) Interface

The USB of WF88-AW supports communication between a host and a device. It is fully compliant with USB 2.0 specifications.

1.7.5 Serial Data (SD) Host Controller

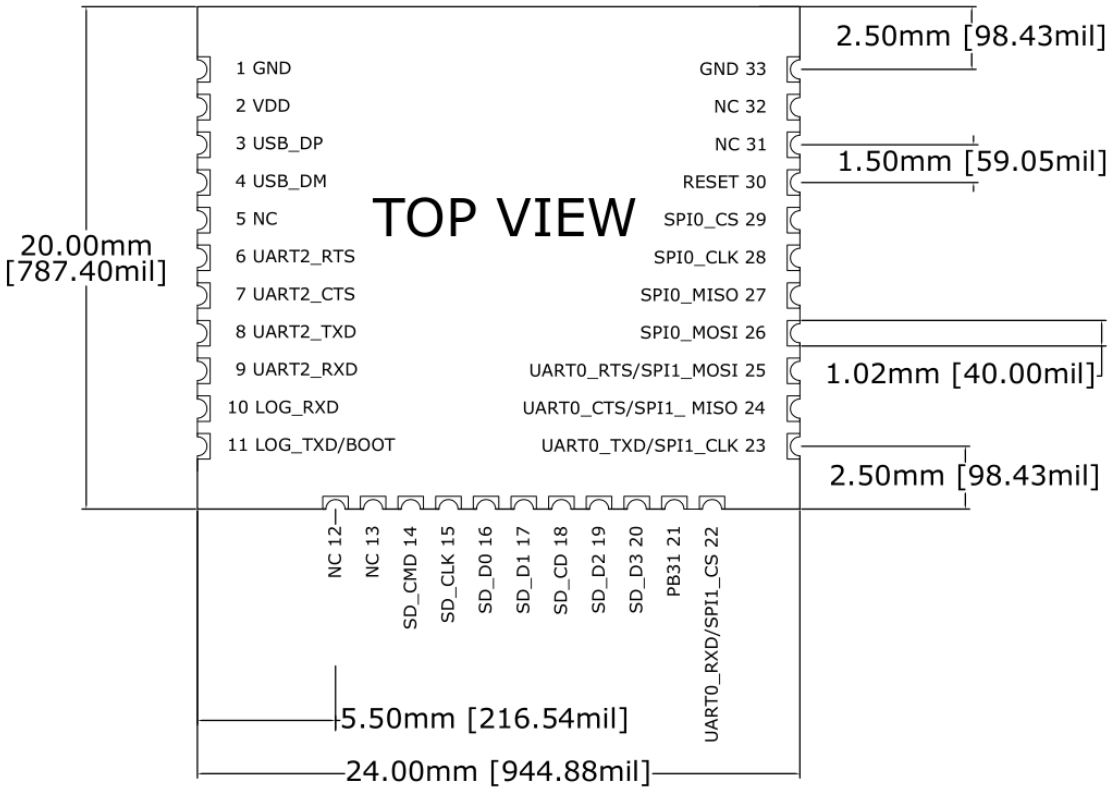
The Serial Data (SD) Host Controller is responsible for accessing SD memory card. It features:

- Compliance with SD memory card specifications version 2.0.
- 1-bit and 4-bit mode
- Default speed mode (25MHz) and High-speed mode (50MHz)
- Card detect with debounce function
- Internal DMA support
- 3.3V operating voltage

2. Module Drawing

Size: 24 mm x 20 mm x 3.05 mm

Top view



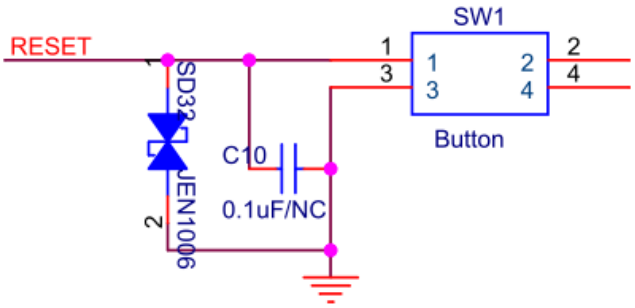
3. Reference Design Circuits

3.1. External Power Supply

- The output voltage of external voltage regulator module can be from 4.5V to 5.5V.
- Continuous output current should be higher than 1A.

3.2. RESET

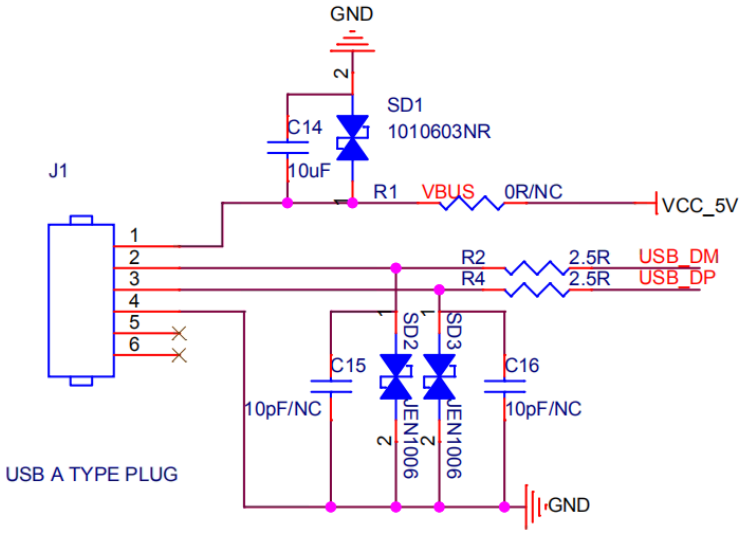
If control by another MCU is needed, please connect directly to external devices. If using key reset, please refer to the figure below.



3.3. SPI

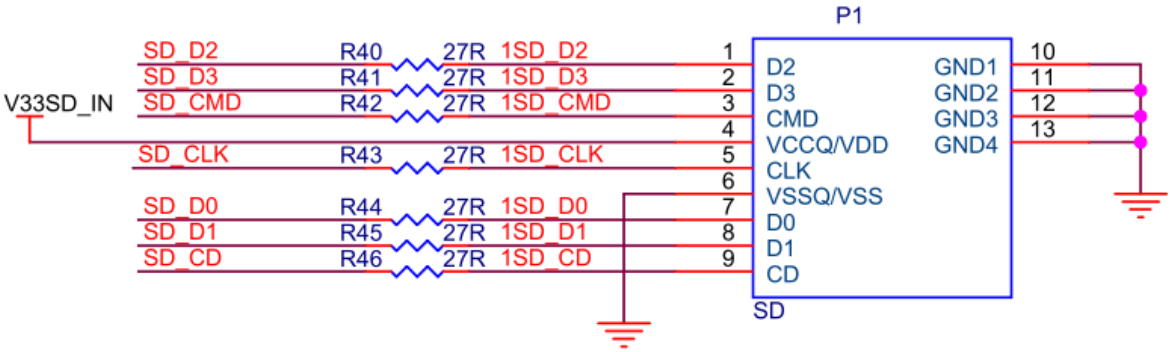
Generally, four signal wires (CS, CLK, MISO, and MOSI) can be directly connected to external device. You can pull CS pin up to VCC by a 10K resistor, so that the CS pin has a certain high level state to avoid bus floating.

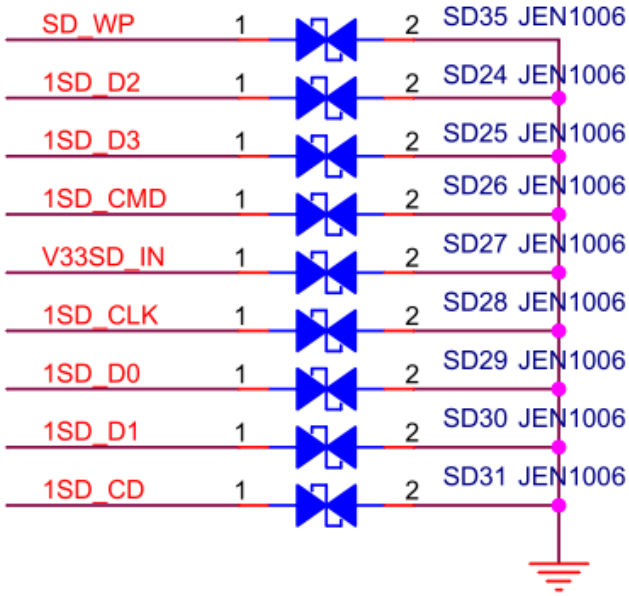
3.4. USB



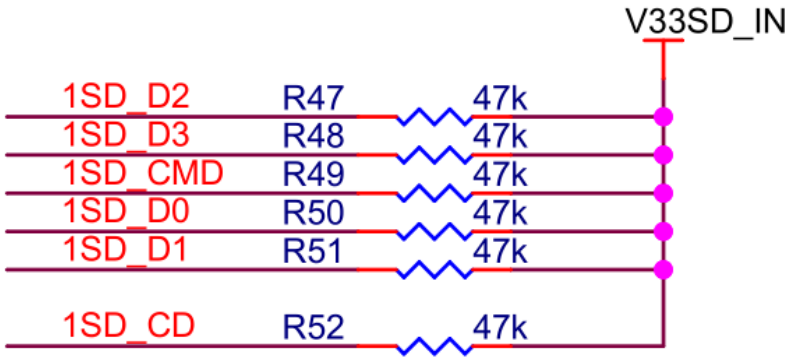
- The VBUS comes from external host. A 10uF filter capacitor should be placed close to the USB interface to reduce the amplitude of power supply spike during plugged in.
- The TVS device should be put closely with USB interface to avoid chip damage caused by ESD.
- The DP/DM is connected in series with a resistor to prevent D+/D- signal overshoot with VBUS. The resistance is generally 2.5 ohm and placed close to the USB interface. It is recommended to reserve a footprint for a capacitor to ground on each trace close to the USB interface.
- DP and DM are wired in a different manner, and through the continuous reference plane layer to ensure the consistency of impedance, the differential impedance of the signal line is Z=90Ω ± 15%.
- The traces of DP and DM must be of the same length, and the length error should not exceed 150mil. Instead of right angles, obtuse angles or arc traces are required. The maximum number of vias is 3, please minimize the use of vias to reduce signal reflection and impedance.

3.5. SD card





- Each SD card cable (power and signal lines) needs to connected to an ESD diode.
- In order to reduce signal distortion and EMI interference, it is recommended to reserve a series damping resistance at the source side on the signal line. The default value is 0 Ω, and the actual resistance value can be adjusted by users according to their needs, usually between 0~47 Ω.The higher the signal rate and the longer the wiring length, the smaller the ideal resistance value. During PCB layout, please place the matched resistance close to the transmitting end.
- The four data cables from D0 to D3, as well as the CMD cable, need to be externally pulled up to IO power. The pull-up resistance is generally between 10K and 100K.



- The VDD of the SD card requires filtering capacitors connected to ground, usually one large and one small capacitor connected in parallel, such as 4.7uF and 0.1uF.

- The data and clock lines should be length-matched and surrounded by ground lines. Ensure that the spacing between lines is greater than three times the line width and reference plane is complete. Avoid placing signal lines close to high frequency signals.

4. Ordering Information

Part Name	Description
WF88-AW	Wi-Fi module, dual band, with U.FL antenna

5. Revision History

Data	Revision	Description
3/26/2026	1.0	Initial release